ABSTRACT OF THE DISCLOSURE

An information processing device which features low power consumption without deterioration in interruption request response speed. It specifies a waiting time until execution of a given event and makes a system call. It comprises: a first timer circuit for a first cycle; a second timer circuit for a second cycle shorter than the first cycle; a timeout supervisor capable of storing the waiting time upon the system call; and a first cycle supervisor capable of storing a time until the next interruption request from the first timer circuit. The timeout supervisor stores the time calculated by subtraction of the time stored in the first cycle supervisor from that in the timeout supervisor upon an interruption request from the first timer; and if the time stored in the timeout supervisor is shorter than the first cycle, the second cycle time is subtracted from the time stored in the timeout supervisor upon an interruption request from the second timer circuit. This reduces power consumption and shortens interruption response time.